

University of California, Santa Barbara
Department of Electrical and Computer Engineering

ECE 152A – Digital Design Principles

Midterm Exam #1
July 18, 2007

Name _____

Perm # _____

Lab Section _____

Problem #1 (20 points) _____

Problem #2 (20 points) _____

Problem #3 (20 points) _____

Problem #4 (20 points) _____

Problem #5 (20 points) _____

Total (100 points) _____

- This is a 75 minute exam; closed book, closed notes, no calculators.
- Answer all questions on the exam.

Problem #1.

For the Boolean expression given below:

$$A(B + C'D) + (BD)'C$$

- a) Using only Boolean algebra, give the equivalent expression in Sum of Products representation (you don't need to simplify the expression).

- b) Enter the function onto a Karnaugh map and identify the prime and essential prime implicants and find a minimal cover in Sum of Products form. Is the minimal cover unique?

- c) Using only Boolean algebra, give the equivalent expression in Product of Sums representation (begin with the minimized Sum of Products representation determined in part b above).

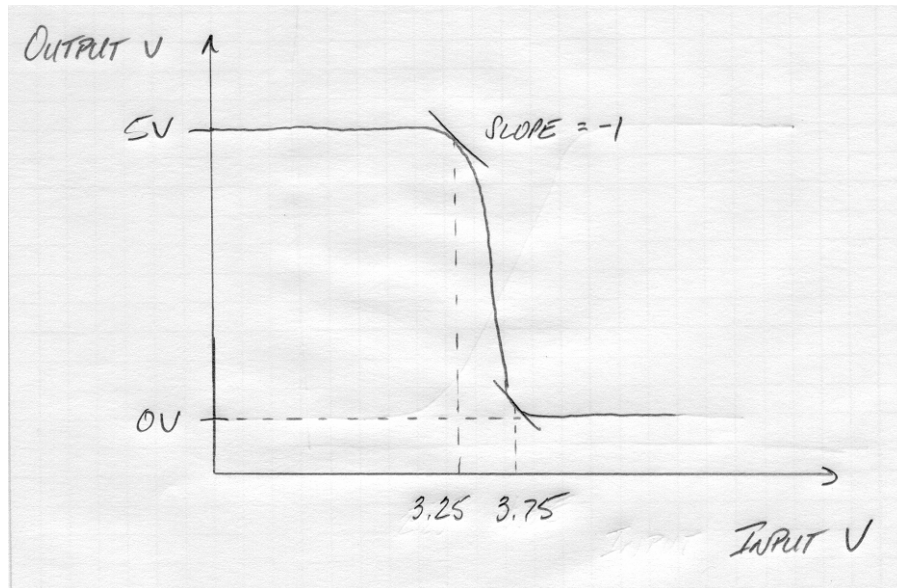
- d) Again enter the function onto a Karnaugh map and identify the prime and essential prime implicants and a minimal cover in Product of Sums form. Is the minimal cover unique?

e) Express the function in canonical sum of minterms form (use the $\sum m (\dots)$ notation).

f) Express the function in canonical product of Maxterms form (use the $\prod M (\dots)$ notation).

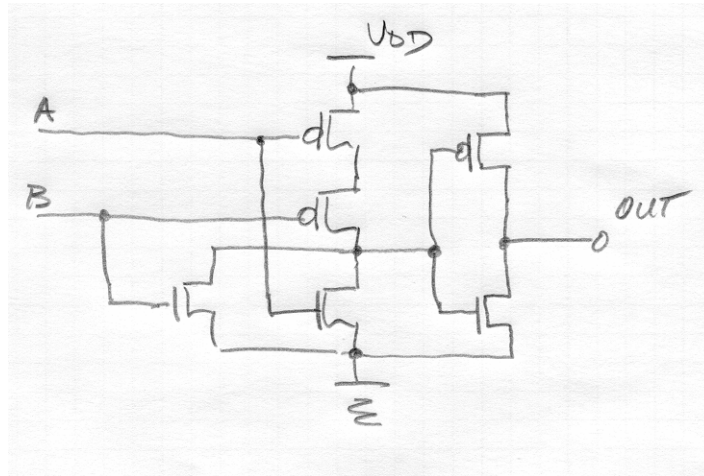
Problem #2.

- a) The figure below illustrates the voltage transfer characteristic (V_{out} vs. V_{in}) for an inverter of unknown technology.



1. What are the numeric values of V_{OH} , V_{IH} , V_{OL} and V_{IL} ?
2. What are the values of the high and low noise margins?

b) What function is realized by the CMOS logic circuit shown below?



- c) Design the CMOS circuit (referred to as a “compound, static gate”) that realizes the function:

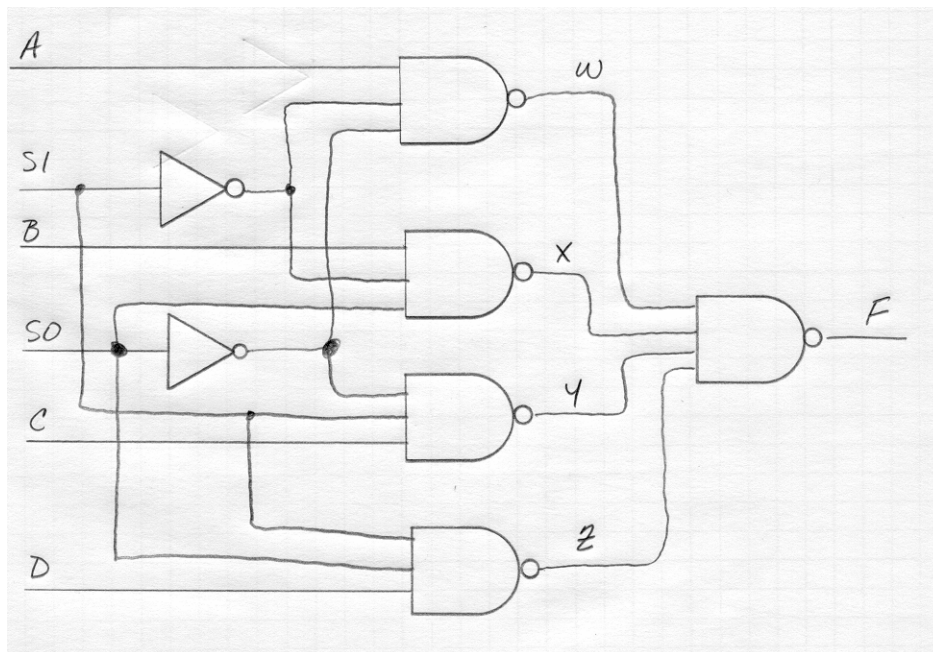
$$A'B' + A'C'$$

Your circuit should use the minimum number of transistors.

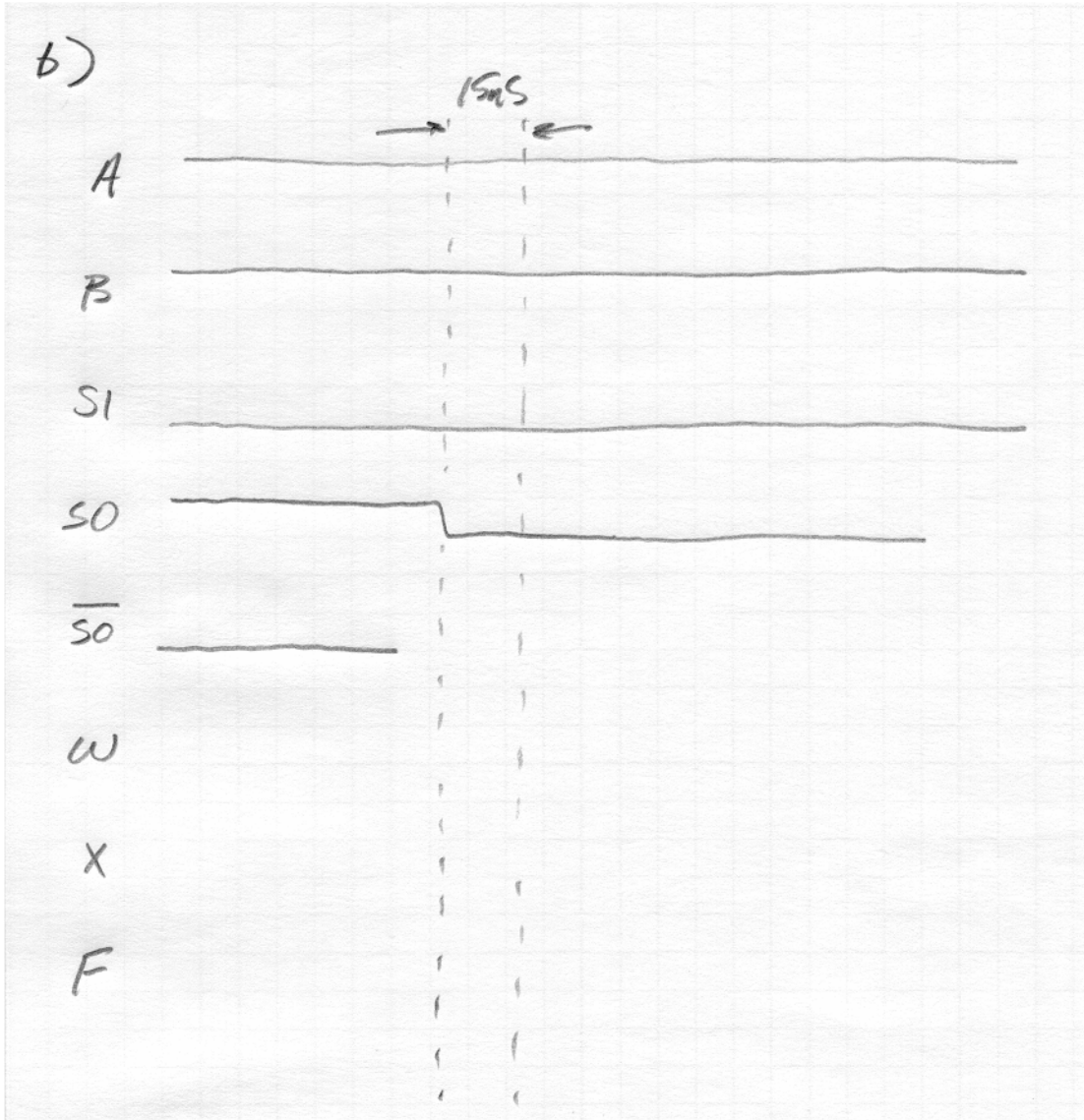
Problem #3.

- a) Identify the critical path and calculate the maximum propagation delay for the circuit shown below. The maximum propagation delays for the gates are:

	t _{plh}	t _{p_{hl}}
Inverter	15ns	20ns
3 input NAND	17ns	22ns
4 input NAND	20ns	25ns



- b) Using the maximum propagation delays from above, complete the timing diagram below. Initial conditions are $A = 1$, $B = 1$, $S1 = 0$ and $S0 = 1$. Indicate all delay times on the timing diagram.



Problem #4.

- a) In this problem, you are asked to design the combinational circuit that examines the contents of a coin box and dispenses Coke[®] and change. The coin box accepts nickels and dimes and dispenses a Coke[®] when it detects 15¢ in the coin box and dispenses a Coke[®] and 5¢ change when it detects 20¢. Once the product and change have been delivered, the coin box is automatically emptied.

The circuit has four inputs, D1D0 (the binary representation of the number of dimes in the coin box) and N1N0 (the number of nickels). The circuit has two outputs K (Coke[®]) and C (change).

Design the circuit and implement it using only NAND gates. Assume you have the following TTL components available:

7400, quad, 2-input NAND gates

7406, hex inverters

7410, triple, 3-input NAND gates

7420, dual, 4-input NAND gates

Implement the circuit using the fewest number of IC's. Draw the schematic and indicate the components being used.

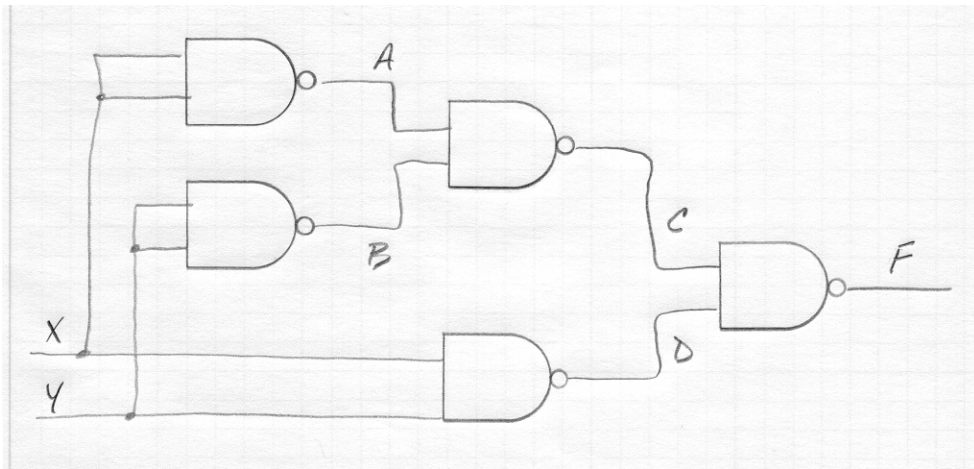
b) Marketing and sales has decided to raise the price of Coke[®] in its vending machines to 20¢ and to allow the machines to also accept quarters. Like the earlier version of the machine, any combination of nickels, dimes and quarters will result in delivery of the product and the appropriate change.

1) How many inputs (bits) will this new circuit require (what determines the contents of the coin box)?

2) How many different values of change (outputs) will this new circuit require?

Problem #5.

For the logic circuit below:



- a) Give the structural (gate level) Verilog code that implements this circuit. Be sure to include all necessary declarations; the syntax doesn't have to be perfect, but all the elements must be present.

- b) Using Verilog's logical operators, rewrite the Verilog code (you don't have to repeat the declarations in this part).